

Table of Contents

Chapter 3:	Single-Transistor and Multiple-Transistor Amplifiers
3.2	Two-Port Modeling of Amplifiers Admittance Parameters, Impedance Parameters, Hybrid Parameter, Inverse Hybrid Parameters, Circuit Representation of Two-Port Networks.
3.3	Basic Single-Transistor Amplifier Stages Small-Signal Model of a BJT, JFET and MOSFET, Common-Emitter Configuration, Common-Source Configuration
3.4	Multiple-Transistor Amplifier Stages Darlington Pair
3.5	Differential Pairs Bartlett's Bisection Theorem, Basic Differential Amplifier, Differential Gain, Common-Mode Gain, Input Resistance, Common-Mode Rejection Ratio, Current Source Biasing
Chapter 3:	Supplemental Problems and Solutions
Chapter 1:	Devices and SPICE Models
1.5	Large-Signal Behavior of MOSFETs Transfer Characteristics, Shichman-Hodges Equations, SPICE Curve Tracer, Large-Signal SPICE Model, Small-Signal Model
1.3	Large-Signal Behavior of Bipolar Transistors Transfer Characteristics, Eber-Moll Equations, Large-Signal SPICE Model, SPICE Curve Tracer, Small-Signal Model
1.X	Large-Signal Behavior of JFETs Transfer Characteristics, Device Equations, SPICE Curve Tracer, Large-Signal SPICE Model, Small-Signal Model
1.Y	FET - BJT Analogy
Chapter 1:	Supplemental Problems and Solutions
Chapter 4:	Current Mirror, Active Loads and References
4.2	Current Mirrors Simple BJT Current Mirror, Model, MOSFET Current Mirror, Design and Simulation, Cascode BJT Current Mirror, Output Resistance, SPICE Verification, Cascode MOSFET Current Mirror, Design and Simulation, Swing Limits, Output Resistance, Wilson BJT Current Mirror, SPICE Verification
4.3	Active Loads Complementary Load, Common-Emitter Amplifier, Common-Source Amplifier, Diode Connected Load - Common Source Amplifier, BJT Differential Pair with Current-Mirror Load, Operating Point, AC Differential Analysis, Symmetry, Output Resistance, Model, AC Common-

	Mode Analysis, Output Resistance, CMRR, Large-Signal Response, CMOS Differential Pair with Current-Mirror Load, Operating Point, AC Differential Analysis, Symmetry, Output Resistance, Model, AC Common-Mode Analysis, Output Resistance, CMRR, Large-Signal Response,
4.4	Voltage and Current References MOSFET Voltage Divider, Design and Simulation, Biasing a Current Mirror
Chapter 4:	Supplemental Problems and Solutions
Chapter 6:	Operational Amplifiers with Single-Ended Outputs
6.8	Bipolar Op-Amps - Intersil 8741 Op-Amp Schematic, SPICE model, DC Transfer Curve, DC Operating Point - Input Stage, Intermediate Stage, Output Stage, Short Circuit Protection, Simulated Small-Signal Gain for Differential and Common-Mode Inputs Small-Signal Model - Input Stage, Intermediate Stage, Output Stage, Overall Model, Offset Adjustment, Transfer Curve with Adjustment, Output Clipping, Frequency Response with and without Dominate Pole Compensation, Stability Criterion, Step Response with and without Dominate Pole Compensation, Dominate Pole Approximation, Slew Rate, Large Signal Step Response
Chapter 7:	Frequency Response of Integrated Circuits
7.X	Large-Signal Model Capacitance NMOS, PMOS, Physical Structure for C_{BX} , C'_{GS} , C'_{GD} , C'_{GB} , NPN, PNP, LPNP
7.2	Single-Stage Amplifiers Common-Source with Active Load - High Frequencies, Open Circuit Time Constant Approximation to Bandwidth
Chapter 9:	Feedback Response and Stability of Feedback Amplifiers
9.X	CMOS Op-Amp Design Differential Amplifier Input Stage, SPICE Testing, Differential Gain, Common-Mode Gain, Small- and Large- Signal Time Domain Response, Differential DC Transfer Curve and Analysis, Common-Mode DC Transfer Curve and Analysis, Common-Source Second Stage and Analysis, Class AB Output Stage with Analysis, Modified Second Stage, Phase Margin, Buffer Instability, Adding a Dominant Pole
9.Y	Characterizing the Op-Amp - Making a Virtual Data Sheet with SPICE DC Transfer Curve, Open-Loop Gain, Output Impedance, Common-Mode Input Range, Common-Mode Gain, CMRR, Short Circuit Current, Slew Rate, Supply Current, Non-inverting Amplifier, Stability - Revisted
9.Z	Analysis and Re-Design Short Circuit Current, Origins of Slew Rate, Re-Design for Stability, Transmission Zero, Replacing the Biasing and Compensating Resistors with MOSFETs, Level 2 Model Parameters, Extracting Level 1 Parameters from Higher Level Models

Chapter 11: Noise in Integrated Circuits

11.3 Noise Models

Input Referenced Noise Model for an Op-Amp, Approximating Peak-to-Peak Noise, Approximating Input Noise using Data Sheet or SPICE Equivalent Input Noise vs Frequency Plots, Thermal Resistor Noise

11.4 Circuit Noise Calculations

Audio Frequency Inverting Amplifier, Restricting Bandwidth to Lower Noise