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Chapter 5: SPICE Components

A. SPICE as a Tool

SPICE Components

Diodes; V-I Characteristics; Reverse Recovery; NPN BJT; V-I Characteristics; PNP BJT; V-I Characteristics; N-Channel JFET; V-I Characteristics; P-Channel JFET; V-I Characteristics; N-Channel MOSFET; V-I Characteristics; P-Channel MOSFET; V-I Characteristics.

Chapter 6: Op Amp Macromodeling

A. Boyle Model

SPICE Test Circuits

Transfer characteristics; Input Bias and Offset Currents; Open Loop Gain; Output Impedance; Common-Mode Gain; Short Circuit Current; Slew Rate

Model Formulas

Input Stage: IC and CE ; SR+; SR-; Jump; Transistor Parameters; Bartlett's Bisection Theorem; One Capacitor Circuits; Input Stage: RCi and REi ; Input Stage: C1 ; Interstage: GCM ; Output Stage: RO1 , RO2 and GB ; Output: Current Limiting; Output: Voltage Limiting; DC Power Drain; Verification.

Design Procedure

Given Op-Amp Parameters, Pick Component Values.

Other Input Stages

PNP Boyle Model; Transfer Characteristics; Slew Rate; Verification; Design Procedure; N-JFET Boyle Model; Transfer Characteristics; Input Stage Changes; Verification; Design Procedure; P-JFET Boyle Model; Transfer Characteristics; Slew Rate; Verification; Design Procedure.

Model Inaccuracies

Device Level Model; Supply Current: Device Level Model; Supply Current: Boyle Model; Supply Current: Device Level Model; Supply Current: Boyle Model; Asymmetric Supplies: Device Level Model; Asymmetric Supplies: Boyle; PSRR: Device Level Model; PSRR: Boyle Model; PSrr+: Device Level Model; PSrr+: Boyle Model; PSrr-: Device Level Model; PSrr-: Boyle Model; Supplies Off: Device Level Model; Supplies Off: Boyle Model; Power Up and Down: Device; Output Impedance: Device; Common-Mode Gain: Device.

B. MicroSim Model

SPICE Test Circuits

Transfer characteristics; Input Bias and Offset Currents; Open Loop Gain; Output Impedance; Common-Mode Gain; Short Circuit Current; Slew Rate; Supply Current; Supply Current During Clipping; Asymmetric Supplies; PSRR; PSrr+; PSrr-; Supplies Off; Power Up and Down.

Model Formulas

Interstage; Input Offset Voltage; Output: Current Limiting; Output: Voltage Limiting; Verification.

Design Procedure

Given Op-Amp Parameters, Pick Component Values.

Other Input Stages

PNP MicroSim Model; Asymmetric Supplies; Verification; Design Procedure; P-JFET MicroSim Model; "Parts" JFET Macromodels; Verification; Design Procedure; N-JFET MicroSim Model; Verification; Design Procedure.

Model Inaccuracies

Asymmetric Supply: Device; Asymmetric Supply: Boyle; Asymmetric Supply: MicroSim; EGND Removed.

Chapter 7: Comparator Macromodeling

A. Getreu Model

SPICE Test Circuits

Transfer characteristics; Response Time: 2 mV OD HL; Response Time: 5 mV OD HL; Response Time: 20 mV OD HL; Response Time: 2 mV OD LH; Response Time: 5 mV OD LH; Response Time: 20 mV OD LH; Strobings

Model Formulas

Input Stage: High-to-Low; Interstage: High-to-Low; Output Stage; Input Stage: Low-to-High; Interstage: Low-to-High; Input Stage; Verification.

Design Procedure

Given Comparator Parameters, Pick Component Values.

Other Output Stages

PNP Getreu Model; Verification; Design Procedure; P-JFET Getreu Model; Verification; Design Procedure.